Remarks

Claims 1-7 are pending.

Claims 1-7 are rejected under 35 U.S.C. §103(a) as being unpatentable over Takagi et al. (US 6,130,458), hereafter "Takagi," in view of Lauffer et al. (EP 0 471 938 A1), hereafter "Lauffer," Wenzel et al. (US 6,150,724), hereafter "Wenzel," and Pogge et al. (US 5,998,868), hereafter "Pogge." This rejection is defective because the cited references, taken alone or in any combination, fail to teach or suggest each and every feature of the present invention as required by 35 U.S.C. §103. In addition, the Examiner has failed to present a *prima facie* case of obviousness in support of the rejection under 35 U.S.C. §103.

Regarding claim 1, Takagi fails to teach or suggest, among other features, a multi-chip module "comprising at least a power semiconductor chip and a control semiconductor chip each mounted directly on an electrically conductive heat sink," wherein "said power semiconductor chip comprises a Silicon-On-Insulator (SOI) device comprising a semiconductor substrate mounted directly on said electrically conductive heat sink, an insulating layer on said semiconductor substrate, an SOI layer on said buried insulating layer, and at least one semiconductor device provided in said SOI layer, wherein each semiconductor device in said SOI layer is electrically insulated from said electrically conductive heat sink by said insulating layer, and wherein said control semiconductor chip comprises a bulk technology semiconductor device having no insulating layer between a device layer and a substrate thereof, and having said substrate connected to ground potential and mounted directly on said electrically conductive heat sink." On the contrary, Takagi discloses a power element chip 200 and a control circuit chip

100, **both formed using SOI technology**, which are mounted on a conductive substrate (see, e.g., FIGS. 12A, 12B; col. 11, line 30-col. 12, line 57).

Takagi is only concerned with power IC's having an SOI structure, and does not teach or suggest providing control circuit chip 100 using a bulk technology semiconductor device having no insulating layer between a device layer and a substrate thereof. Takagi discloses a plurality of different embodiments of SOI power IC's, each including SOI control and power structures that have been specifically designed to prevent/inhibit the problems of latchup and leakage current present in prior art SOI power IC's. Thus, one of ordinary skill in the art would not be motivated to use a bulk semiconductor device to implement Takagi's control circuit chip 100.

In order to overcome this glaring deficiency of Takagi, the Examiner presents a convoluted argument involving the disparate teachings of Lauffer, Wenzel and Pogge in an attempt to prove that it "would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a control semiconductor chip comprising a bulk technology device and an electrically conductive heat sink substrate connected to ground potential as taught by Lauffer et al. so that heat dissipation, temperature distribution and power requirement can be improved in Wenzel et al., and Pogge et al. and Takagi et al's multichip module." Applicants respectfully disagree with the Examiner's analysis and conclusion.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success.

Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Applicants submit that there is no suggestion or motivation to modify Takagi in the manner suggested by the Examiner.

Takagi discloses the formation of monolithic and hybrid power integrated circuits (IC's) using SOI technology. In particular, as detailed above, Takagi discloses a plurality of different embodiments of SOI power IC's, each including SOI control and power structures that have been specifically designed to prevent/inhibit the problems of latchup and leakage current present in prior art SOI power IC's. Takagi is concerned only with problems associated with SOI power IC's, and is not concerned in any way with bulk semiconductor devices. As such, one of ordinary skill in the art would not be motivated to modify Takagi to include a control circuit chip formed using a bulk semiconductor technology as asserted by the Examiner. Indeed, this modification would likely render Takagi inoperable for its specific intended purpose, i.e., the prevention of latchup and the reduction of leakage current present in prior art SOI power IC's.

Takagi does not teach or suggest that the disclosed SOI power ICs have a problem with heat dissipation or temperature distribution. Accordingly, one of ordinary skill in the art would not be motivated to directly mount the SOI power structures on an electrically conductive heat sink as set forth in claim 1. While Takagi does disclose mounting the SOI power structures on a thin, electrically conductive substrate 81 (FIG. 12B), the substrate 81 is provided only to bias the p-type silicon substrate 11, 91 (FIG. 12B) to ground, and is not provided for heat dissipation.

The Examiner alleges that "Lauffer et al. teach using a multichip module having a variety

of chips such as high power, low power, memory, logic chip, etc. in the same package being directly mounted on the electrically conductive heat sink/substrate made of copper (11 in Fig. 4; Col. 9, line 7) which is connected to a ground potential (Col. 12, line 32)." This is incorrect. On the contrary, in Lauffer, only a single high power integrated circuit chip 112 is disclosed as being mounted directly to heat sink/ground plane 11. As is clearly shown in FIG. 4 of Lauffer, high power integrated circuit chip 113 and low power logic and/or memory integrated circuit chip 115 are separated and insulated from heat sink/ground plane 11 by a layer of a dielectric 14.

The Examiner alleges that "Wenzel et al. teach using a multichip module (Fig. 5-8) having a chip/mother chip being connected to a single or multilayer conductor substrate having no insulating layer between the device/device layer and the substrate (106a in Fig. 5-8; Col. 5, line 63), the substrate having a heat sink structure for improving heat dissipation (Col. 7, line 50 – Col. 8, line 10)." This is incorrect. In particular, in FIGS. 5-8 of Wenzel et al., only the mother chip 102 is shown "mounted" via connection bumps 110 to package 106; the daughter chip 104 is suspended above the package.

It should also be noted that in the claimed invention, SOI and bulk semiconductor **devices**, not chips, are mounted directly to an electrically conductive substrate. Lauffer, Wenzel, and Pogge each disclose the attachment of chips to a substrate, and do not disclose the mounting of semiconductor devices within the chips to a substrate. Accordingly, there is no motivation to combine such chip level mounting schemes of Lauffer, Wenzel, and Pogge with the SOI structure of Takagi.

Accordingly, because the cited references, taken alone or in any combination, fail to

teach each and every feature of claim 1, Applicants respectfully submit that claim 1 is allowable.

Claims 2-7 depend from independent claim 1, and are, therefore, patentable for at least the reasons set forth above.

If the Examiner believes that anything further is necessary to place the application in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number listed below.

Respectfully submitted,

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John A. Merecki
Reg. No. 42,456

Hoffman, Warnick & D'Alessandro LLC
Three E-Comm Square
Albany, NY 12207
(518) 449-0044 - Telephone
(518) 449-0047 - Facsimile